HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200208858-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Samuel D. Naffziger, et al. **Confirmation No.:**

Application No.: **Examiner:**

Filing Date: **Group Art Unit:**

Title: SYSTEM AND METHOD TO ADJUST VOLTAGE

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97(c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **EU853429629US**

Date of Deposit **August 26, 2003**

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By

Typed Name: **Lisa D. Jones**

Respectfully submitted,

Samuel D. Naffziger, et al.

By

Gary J. Pitzer

Attorney/Agent for Applicant(s)
Reg. No. **39,334**

Date: **August 26, 2003**

Telephone No.: **(216) 621-2234**

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use sev ral sheets if nec ssary)	ATTY. DOCKET NO. **200208858-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Samuel D. Naffziger, et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	2003/0060176	03/27/2003	Heinonen, et al.	
	1B	6,157,247	12/05/2000	Abdesselem, et al.	
	1C	6,449,575 B2	09/10/2002	Bausch, et al.	
	1D	6,509,788 B2	01/21/2003	Naffziger, et al.	
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	THOMAS D. BURD, et al., "A Dynamic Voltage Scaled Microprocessor System", IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, pp. 1571-1580, November 2000
	1R	SHEKHAR BORKAR, et al., "Parameter Variations and Impact on Circuits and Microarchitecture", Circuit Research, Intel Labs, JF3-334, pp. 338-342, June 2003
	1S	

EXAMINER	DATE CONSIDERED